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10/821,054	04/08/2004	Susan E. Eisen	AUS920031069US1	9646

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EXAMINER	
ZALEPA, GEORGE D	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,054	EISEN ET AL.	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,13,15,21,22,29 and 31* is/are rejected.

7)☒ Claim(s) *7-12,14,16-20,23-28,30 and 32-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/08/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-36 have been considered by the examiner.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

a. Declaration as Filed on 8 April 2004

b. Information Disclosure Statement as filed on 8 April 2004

c. Replacement drawings filed 16 July 2004

Information Disclosure Statement

3. The references listed in the Information Disclosure Statement submitted on 8 April 2004 have been considered by the examiner (see attached PTO-1449).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 6-20 are objected to because of the following informalities: In lines 4-5, Applicant refers to selecting an identification of "one of an instruction finished **and** an instruction active". Emphasis added. In lines, 6-7 Applicant refers to calculating an identification based on one selected instruction ("using said identification of said selected instruction"). Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1 and 3 are rejected under 35 U.S.C. 102(a) as being anticipated by Kahle et al. (US Pat. No. 6,654,869; herein referred to as "Kahle").

8. Regarding **independent claim 1**,

9. Kahle discloses *a completion table* [see Kahle, Fig. 1, element 118], *comprising: a plurality of entries* [see Kahle, Fig. 2, elements 202a, 202b], *wherein each of said plurality of entries tracks a consecutive number of outstanding instructions* [see Kahle, Fig. 2, correspondence between consecutive instructions in element 201 and instruction grouped instructions 204a-e], *wherein each of said plurality of entries is configured to store an instruction address of a first of said consecutive number of outstanding instructions and an identification of said first of said consecutive number of outstanding instructions* [see Kahle, Fig. 2, element "GTAG"].

10. Regarding **claim 3**,

11. Kahle discloses *the completion table as recited in claim 1, wherein said instruction address is an effective address* [see Kahle, Col. 6, lines 58-60; Examiner's note: Kahle discloses the instruction address corresponding to the first instruction of the group thus an effective address, as it does not address the instructions after directly.].

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 2 is rejected under 35 U.S.C. 103(a) as being obvious over Kahle.

14. Regarding **claim 2**,

15. Kahle discloses the limitations as stated in **independent claim 1**.

16. Kahle does not explicitly disclose *said consecutive number of outstanding instruction* [comprising] *a cache line*.

17. However, in Fig. 2 of Kahle, Kahle shows a sequence of instructions being stored in one completion table entry. It would have been an obvious advantage to create the completion table lines to be the same length as the cache lines as it would increase the coherency of the completion table. By forcing the completion table to be the same size as the cache, one would eliminate the problem of splitting cache lines and therefore would reduce the amount of logic required to issue instructions to the completion table. Furthermore, Kahle uses a group tag which corresponds to a grouping of executable instructions. It would have been obvious to one of ordinary skill in the art at the time of invention that the most logical group would be the cache line group that the instructions are in when received from memory.

18. Claims 4-6, 13, 15, 21-22, 29 and 31 are rejected under 35 U.S.C. 103(a) as being obvious over Song (US Pat. No. 5,546,599; herein referred to as "Song") in view of Kahle and in view of Siedl et al (US Pat. No. 6,751,709; herein referred to as "Siedl").

19. Regarding **claim 4**,

20. Kahle discloses the limitations as stated in **independent claim 1**.

21. Kahle does not disclose *an instruction address and an identification of a next to complete instruction is calculated using said instruction address of said first of said consecutive number of*

outstanding instructions and said identification of said first of said consecutive number of outstanding instructions, respectively, in a selected entry of said completion table.

22. Siedl does disclose *an instruction address and an identification of a next to complete instruction is calculated using said instruction address of said first of said consecutive number of outstanding instructions and said identification of said first of said consecutive number of outstanding instructions, respectively, in a selected entry of said completion table* [see Siedl, Col. 4, lines 18-23; Examiner's note: Siedl discloses using an address and ID to compute a physical address to translate the address and ID to a usable address.].

23. Kahle does not disclose a method of determining a next to complete instruction within a completion table by calculating the address based on a group tag and first instruction address. Kahle discloses ungrouping the instruction groups when an access to an instruction within a group is needed. Siedl discloses a method of receiving a tag and first address and computing a physical address of an instruction based on said tag and first address. The advantage of calculating an address of an instruction within the group rather than ungrouping and re-executing the instruction would have been to minimize the complexity of the reorder buffer operations within the processor. It would have been obvious to one of ordinary skill in the art at the time of invention that un-grouping and re-entering the instructions into the reorder buffer would have been a considerably more complex operation than calculating the instruction within the group based on information (group tag and address) that already existed within the group. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the grouped reorder buffer disclosed by Kahle with the goal of decreasing processor size and the instruction calculating technique, as disclosed by Siedl, to decrease the complexity of the selection mechanism compared to the ungroup and reissue scheme disclosed by Kahle.

24. Regarding **claim 5**,

25. Kahle and Siedl disclose the limitations as stated in **claim 4**.

26. Regarding **independent claim 6**,

27. Song discloses *a method for tracking a larger number of outstanding instructions in a completion table comprising the steps of: issuing instructions to a first and a second execution unit* [see Song, Col. 1, lines 26-28]; *selecting an identification of one of an instruction finished and an instruction active at one of said first and said second execution unit* [see Song, Col. 8, lines 6-8; lines 13-16; Examiner's note: Song discloses a reorder buffer (Fig. 6) containing a finished flag for all instructions (those in flight (finished=0) and those finished (finished=1)), in lines 6-8, Song discloses a completion unit reading the entries of the reorder buffer to determine completion status, thus reading both finished and executing instructions and selecting of them instructions to complete (Col. 8, lines 16-18).]; *calculating an identification of a next to complete instruction using said identification of said selected instruction* [see Song, Col. 8, lines 21-34; Examiner's note: Song discloses the criteria for an instruction to be marked for completion, thus given the structure of the reorder buffer, it is clear that Song selects the data from the reorder buffer (finished=1) and calculates which of the instructions is to be finished.].

28. Song does not disclose *selecting an instruction address and an identification of a first of a consecutive number of outstanding instructions located in an entry of said completion table; and calculating an instruction address of said next to complete instruction using said identification of said next to complete instruction and said selected instruction address and identification of said first of said consecutive number of outstanding instructions located in said entry of said completion table.*

29. Kahle does disclose *selecting an instruction address and an identification of a first of a consecutive number of outstanding instructions located in an entry of said completion table* [see Kahle, Col. 5, lines 57-59 (identification); Col. 6 line 65 to Col. 7, line 1 (instruction address)].

30. Kahle and Song do not disclose *calculating an instruction address of said next to complete instruction using said identification of said next to complete instruction and said selected instruction address and identification of said first of said consecutive number of outstanding instructions located in said entry of said completion table.*

31. Siedl does disclose *calculating an instruction address of said next to complete instruction using said identification of said next to complete instruction and said selected instruction address and identification of said first of said consecutive number of outstanding instructions located in said entry of said completion table* [see Siedl, Col. 4, lines 18-23; Examiner's note: Siedl discloses using an address and ID to compute a physical address to translate the address and ID to a usable address.].

32. Song discloses a method of tracking instructions that are finished and active in a processor. Song also utilizes the reorder buffer to determine when to retire instructions based on selected an instruction out of instructions that are active (finished=0) and are finished (finished =1). Song does not disclose the reorder buffer storing instructions in a line; rather, Song discloses the reorder buffer storing one instruction per line. Kahle does disclose instructions being allocated in a cache-like fashion, with a group tag and first instruction address stored as an identification of the completion table line (Kahle, Fig. 4). The advantage of utilizing a reorder buffer (completion table) that maintains a line of instructions as opposed to the reorder buffer of Song that stores individual instructions on a line would have been to minimize the amount of space needed by the reorder buffer while maintaining an accurate representation of instructions within the processor. As shown by Kahle, in figure 4, two identical instruction groups would require six slots in a group scheme (top figure of figure 4) and would require twelve slots in a non-grouped scheme. Thus, grouping the instructions within the reorder buffer would allow one to minimize the space used by Song and thus decrease the overall size of the processor. Kahle does not disclose a method of determining a next to complete instruction within a completion table by

calculating the address based on a group tag and first instruction address. Kahle discloses ungrouping the instruction groups when an access to an instruction within a group is needed. Siedl discloses a method of receiving a tag and first address and computing a physical address of an instruction based on said tag and first address. The advantage of calculating an address of an instruction within the group rather than ungrouping and re-executing the instruction would have been to minimize the complexity of the reorder buffer operations within the processor. It would have been obvious to one of ordinary skill in the art at the time of invention that un-grouping and re-entering the instructions into the reorder buffer would have been a considerably more complex operation than calculating the instruction within the group based on information (group tag and address) that already existed within the group. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the grouped reorder buffer disclosed by Kahle with the goal of decreasing processor size and the instruction calculating technique, as disclosed by Siedl, to decrease the complexity of the selection mechanism compared to the ungroup and reissue scheme disclosed by Kahle.

33. Regarding **claim 13**,

34. Song, Kahle and Siedl disclose the limitations as stated in independent claim 6.

35. Song further discloses *said selected instruction* [being] *a most recently finished instruction at one of said first and said second execution unit* [see Song, Col. 8, lines 21-34; Examiner's note: In the invention disclosed by Song, it is clear that a most recently finished instruction could be the selected instruction if it is compared to a active instruction which is not ready for completion.].

36. Regarding **claim 15**,

37. Song, Kahle and Siedl disclose the limitations as stated in independent claim 6.

38. Song further discloses *said first execution unit* [being] *a floating point unit* [see Song, Fig. 1, element 30], *wherein said second execution unit* [being] a fixed point unit [see Song, Fig. 1, element 22].

39. Regarding **claims 21-22**,

40. Song discloses *a processor, comprising: an instruction fetch unit configured to fetch instructions* [see Song, Fig. 1, element 14; Examiner's note: It is clear that instructions must be fetched by the instruction cache from memory 39]; *an instruction dispatch unit coupled to said instruction fetch unit* [see Song, Fig. 1, element 18; Fig. 3], *wherein said instruction fetch unit is further configured to issue said fetched instructions to said instruction dispatch unit* [see Song, Col. 2, lines 59-61], *wherein said instruction dispatch unit comprises an instruction queue* [see Song, Fig. 3, element 70] *configured to store said fetched instructions* [see Song, Col. 7, lines 16-20]; *a first and a second execution unit coupled to said instruction dispatch unit* [see Song, Fig. 1, elements 22 and 30], *wherein said dispatch unit is configured to dispatch said stored fetched instructions to said first and said second execution unit* [see Song, Col. 7, lines 23-26]; *and a completion unit coupled to said instruction fetch unit* [see Song, Fig. 3, element 76].

41. Kahle discloses *issuing an instruction address and an identification of each of said fetched instructions to said completion unit* [see Kahle, Col. 5, lines 40-43; Fig. 3; Examiner's note: Kahle discloses tracking issued instructions with in a completion unit. The completion unit in figure 3 illustrates the use of a group identification and an instruction address, thus it is clear that these two values are transmitted to the completion unit for each instruction.], *wherein said completion unit is configured to keep track of when said fetched instructions have been completed* [see Kahle, Col. 5, lines 40-43; Examiner's note: By definition unit, a completion unit functions to keep track of when instructions are completed.].

42. Kahle also discloses *a completion table* [see Kahle, Figs. 3-4], *wherein said completion table comprises a plurality of entries* [see Kahle, Fig. 3, elements 302a, 302n], *wherein each of said plurality of entries tracks a consecutive number of outstanding instructions* [see Kahle, Fig. 2, correspondence between program 201 and instructions 204a-e in first example], *wherein each of said plurality of entries is configured to store an instruction address* [see Kahle, Fig. 4, element

210] *of a first of said consecutive number of outstanding instructions and an identification of said first of said consecutive number of outstanding instructions* [see Kahle, Fig. 4, element 208].

43. Song further discloses *logic for selecting an identification of one of an instruction finished and an instruction active at one of said first and said second execution unit* [see Song, Col. 8, lines 21-34; Examiner's note: Song discloses the criteria for an instruction to be marked for completion, thus given the structure of the reorder buffer, it is clear that Song selects the data from the reorder buffer (finished=1) and calculates which of the instructions is to be finished.].

44. Kahle further discloses *logic for calculating an identification of a next to complete instruction using said identification of said selected instruction; logic for selecting an instruction address and an identification of a first of a consecutive number of outstanding instructions located in an entry of said completion table* [see Kahle, Col. 5, lines 57-59 (identification); Col. 6 line 65 to Col. 7, line 1 (instruction address)].

45. Siedl further discloses *logic for calculating an instruction address of said next to complete instruction using said identification of said next to complete instruction and said selected instruction address and identification of said first of said consecutive number of outstanding instructions located in said entry of said completion table* [see Siedl, Col. 4, lines 18-23; Examiner's note: Siedl discloses using an address and ID to compute a physical address to translate the address and ID to a usable address.].

46. **Claims 21-22** are rejected as being the apparatus performing the method of **claim 6**.

47. Song discloses a method of tracking instructions that are finished and active in a processor. Song also utilizes the reorder buffer to determine when to retire instructions based on selected an instruction out of instructions that are active (finished=0) and are finished (finished =1). Song does not disclose the reorder buffer storing instructions in a line; rather, Song discloses the reorder buffer storing one instruction per line. Kahle does disclose instructions being allocated in a cache-like fashion, with a group tag and first instruction address stored as an identification of the

completion table line (Kahle, Fig. 4). The advantage of utilizing a reorder buffer (completion table) that maintains a line of instructions as opposed to the reorder buffer of Song that stores individual instructions on a line would have been to minimize the amount of space needed by the reorder buffer while maintaining an accurate representation of instructions within the processor. As shown by Kahle, in figure 4, two identical instruction groups would require six slots in a group scheme (top figure of figure 4) and would require twelve slots in a non-grouped scheme. Thus, grouping the instructions within the reorder buffer would allow one to minimize the space used by Song and thus decrease the overall size of the processor. Kahle does not disclose a method of determining a next to complete instruction within a completion table by calculating the address based on a group tag and first instruction address. Kahle discloses ungrouping the instruction groups when an access to an instruction within a group is needed. Siedl discloses a method of receiving a tag and first address and computing a physical address of an instruction based on said tag and first address. The advantage of calculating an address of an instruction within the group rather than ungrouping and re-executing the instruction would have been to minimize the complexity of the reorder buffer operations within the processor. It would have been obvious to one of ordinary skill in the art at the time of invention that un-grouping and re-entering the instructions into the reorder buffer would have been a considerably more complex operation than calculating the instruction within the group based on information (group tag and address) that already existed within the group. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the grouped reorder buffer disclosed by Kahle with the goal of decreasing processor size and the instruction calculating technique, as disclosed by Siedl, to decrease the complexity of the selection mechanism compared to the ungroup and reissue scheme disclosed by Kahle.

48. Regarding **claim 29**,

49. Song, Kahle, and Siedl disclose the limitations as stated in **claim 22**.

50. Song further discloses *said selected instruction* [being] *a most recently finished instruction at one of said first and said second execution unit* [see Song, Col. 8, lines 21-34; Examiner's note: In the invention disclosed by Song, it is clear that a most recently finished instruction could be the selected instruction if it is compared to a active instruction which is not ready for completion.].

51. Regarding **claim 31**,

52. Song, Kahle, and Siedl disclose the limitations as stated in **claim 22**.

53. Song further discloses *said first execution unit* [being] *a floating point unit* [see Song, Fig. 1, element 30], *wherein said second execution unit* [being] a fixed point unit [see Song, Fig. 1, element 22].

Allowable Subject Matter

54. Claims 7-12, 14, 16-20, 23-28, 30 and 32-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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